REMARKS/ARGUMENTS

Claims 1-2, 7-8 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Furukawa et al., US patent No. 6,333,533. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa in view of Alsmeier US patent No. 5,867,420. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa in vie of admitted prior art.

1. **Interview summary:**

A telephone interview was conducted between US Patent Agent Scott Margo (Reg. # 56,277) and Examiner Samuel Gebremariam on June 1st, 2005. Claim 1 was discussed.

Mr. Margo asked the Examiner to clarify how the Furukawa et al. patent (US 6,333,533) teaches a first isolation portion covering the conductive layer of the trench capacitor, as is recited in claim 1. The Examiner stated that a first isolation portion 75 covers the electrode 69, and these two structures teach this claim limitation. The Examiner continued by saying that the language of claim 1 does not contain any limitations that preclude the Examiner from using the gate electrode 69 as a conductive layer of the trench capacitor structure.

2. **Rejection of claims 1-2, 7-8, and 19 under 35 U.S.C. 102(b):**

Claims 1-2, 7-8 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Furukawa et al., US patent No. 6,333,533, for reasons of record that can be found on pages 2-4 in the Office action identified above.

Response:

To overcome the rejection, claim 1 is amended for clearly defining the characteristics of the isolation structure. No new matter is introduced. The amended

claim 1 is listed as below with a clean version:

"An isolation structure of a trench capacitor, the trench capacitor being disposed in a deep trench of a substrate and comprising:

a storage node serving as a top plate of the capacitor in the deep trench;

a bottom plate buried in the substrate around the deep trench;

a capacitor dielectric layer positioned between the storage node and the bottom plate, on a sidewall of the deep trench, the storage node, *the bottom plate, and the capacitor dielectric forming a storage capacitance*; and

a collar oxide layer disposed on the sidewall of the deep trench, the isolation structure comprising:

a first isolation portion *directly contacting and completely covering the top surface of the storage node to separate and isolate the storage node from other conductive elements positioned* above the storage node, the first isolation portion *completely filling a top opening of the deep trench* and having a first thickness; and

a second isolation portion directly contacting the first isolation portion and surrounding the deep trench without overlapping the deep trench, the second isolation portion having a second thickness larger than the first thickness, the second isolation portion *directly contacting and positioned beside and adjacent to both a top portion of the storage node and a top portion of the collar oxide layer*."

Accordingly to the amended claim 1, an isolation structure for isolating a trench capacitor includes a first isolation portion and a second isolation portion. *The first isolation portion directly contacts the storage node and completely covers the whole top surface of the storage node*, wherein the storage node forms a storage capacitance with a bottom plate and a capacitor dielectric. In addition, *the second isolation portion directly contacts the top portions of the storage node and the collar oxide layer side by side.*

Regarding to the application of Furukawa et al., they teach a structure including a vertical transistor, a trench capacitor, and a silicon dioxide collar 59 positioned in a deep trench, wherein the trench capacitor has an n+ polysilicon (storage node

electrode) 57, a node dielectrics 55, and a n+ buried plate 53 forming a capacitance together (Fig, 10, col.4, lines 8-15, lines 49-59). According to col.5, lines 41-55, and Fig.9, the n+ polysilicon 69 formed on the HDP oxide layers 65 and beside the gate dielectric 67 functions as a gate conductor of Furukawa's vertical transistor. Since *a gate of a vertical transistor is always separated and isolated from the capacitor in a usual DRAM device, the gate conductor 69 is also separated from the storage node electrode 57 and certainly does not belong to the trench capacitor*. On the other hand, the Examiner mentioned the isolation structure 75 of Furukawa has a first isolation portion having a first thickness and a second isolation portion having a second thickness larger than the first thickness. According to Fig.10 and the specification of Furukawa et al., *the first isolation portion of Furukawa is positioned above the **gate conductor 69** without completely covering the top surface of the gate conductor 69*, while it is the conductor 77 that covers most top surface of the gate conductor 69. Therefore, *the first isolation portion of isolation structure 75 never directly contacts **the storage node electrode 57** nor completely covers the whole top surface of the **storage node electrode 57***.

In another aspect, the second isolation portion of *the isolation structure 75*, mentioned by the Examiner, is positioned *beside the gate conductor 69, but not beside and adjacent to the silicon dioxide collar 59 or the storage node electrode 57*. In contrast, the second isolation portion of the isolation structure 75 is positioned far above the silicon dioxide collar 59 without contact. Therefore, *Furukawa et al. never teach forming the second isolation portion of structure 75 that contacts the silicon dioxide collar 59 and the storage node electrode 57 nor teach that the second isolation portion is positioned beside and adjacent to the silicon dioxide collar 59 and the storage node electrode 57*.

To sum up, Furukawa et al. do not disclose all the limitations that define the relative position and structure of the first and second isolation portions in the amended claim 1 of the present application. Therefore, the amended claim 1 should be allowable. Reconsideration of the amended claim 1 is thereby politely requested.

Claims 2, and 7-8 are dependent upon the amended claim 1. Therefore, they should be allowable if the amended claim 1 is allowable. Reconsideration of claims 2, 7-8 is hereby requested. Claim 19 is canceled and merged into the amended claim 1. Sequentially, no consideration of claim 19 is needed anymore.

3. Rejection of Claims 4-6 under 35 U.S.C. 103(a):

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa in view of Alsmeier US patent No. 5,867,420, for reasons of record that can be found on pages 4-5 in the Office action identified above.

Response:

Since claims 4-6 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowable. Reconsideration of claims 4-6 is hereby requested.

4. Rejection of Claims 3 under 35 U.S.C. 103(a):

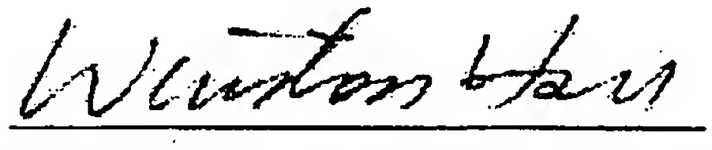
Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa in view of admitted prior art, for reasons of record that can be found on pages 5-6 in the Office action identified above.

Response:

Claim 3 is amended to define that *the bottom of the second isolation portion is lower than the top of the collar oxide layer which is contacted by the second isolation portion*. Referring Fig.11 of the present application, the top of the collar oxide layer that contacts the second isolation portion is at the same plane of the boundary of the numerals 61 and 60. Since claim 3 is dependent upon claim 1, it should be allowed if the amended claim 1 is allowable, Reconsideration of the amended claim 3 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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